CLAIMS

1. A flash memory device formed from a substrate, the device comprising:

strings of transistors of a NAND architecture comprising a first select gate, a plurality of floating gates, and a second select gate,

each floating gate having at least two sides perpendicular to the axes of the strings;

a conductive isolating member adjacent to each of the at least two perpendicular sides of the floating gate and located between adjacent transistors in the strings of transistors, each isolating member shielding a selected floating gate from a charge stored in an adjacent component.

2. The flash memory device of claim 1, wherein the floating gates are formed between shallow trench isolation areas and wherein the device further comprises wordlines extending across adjacent strings and extending between the floating gates into the shallow trench isolation areas thereby isolating adjacent floating gates.

3. The flash memory device of claim 1 wherein the isolating members have two principal faces, the faces substantially parallel to the at least two sides of each floating gate and substantially perpendicular to the axes of the strings.

4. The flash memory device of claim 1 wherein the isolating members extend a distance between the substrate and an upper level of the floating gates.

5. The flash memory device of claim 4 wherein the floating gates have an upper level and a lower level, the isolating members extending from the substrate a distance between the lower and upper level.

6. The flash memory device of claim 1, wherein the isolating members and the wordlines comprise a conductive material, and wherein the isolating members are electrically connected to a wordline above a floating gate that the isolating members shield.

7. The flash memory device of claim 6 wherein the floating gates are approximately T shaped, and wherein isolating members electrically coupled to the wordlines flank the floating gates.

8. The flash memory device of claim 1 wherein the isolating members shield a floating gate of the plurality of floating gates from an electrical field of an adjacent floating gate, thereby minimizing field effect coupling between adjacent floating gates.

9. The flash memory device of claim 8 wherein the adjacent floating gate is diagonally adjacent or horizontally adjacent to the selected floating gate and wherein the isolating members further minimize field effect coupling in the wordline direction.

10. A non-volatile memory device comprising:

floating gates that store a charge;

bitlines that select amongst the floating gates, each bitline having a bitline axis;

wordlines that select amongst the floating gates; and

sidewall elements positioned along the bitline axes, the sidewall elements located at sides of the floating gates between adjacent floating gates, the sidewall elements shielding the floating gates.

11. The memory device of claim 10 wherein the sidewall elements shield the floating gates from an electrical field having a component in the direction of the bitline axes.

12. The memory device of claim 10 wherein the sidewall elements extend from the substrate to the floating gates.

13. The memory device of claim 12 wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the lowermost surface.

14. The memory device of claim 12 wherein the floating gates have an uppermost and a lowermost surface, the sidewall elements extending from the substrate until or beyond the level of the uppermost surface.

15. The memory device of claim 10 wherein the sidewall elements comprise a conductive material and wherein the sidewall elements are electrically coupled to a wordline located between adjacent pairs of sidewall elements.

16. The memory device of claim 15 wherein the coupled sidewalls effectively increase the surface area of the wordline and the electrical coupling between the wordline and the floating gates, thereby aiding in read and write operations.

17. The memory device of claim 10 wherein the wordlines extend between adjacent floating gates so as to shield a selected floating gate from an electrical field of adjacent floating gates, and wherein the non-volatile storage device is NAND flash memory.

18. A method of forming NAND flash memory comprising:

forming floating gates;

forming control gates above the floating gates;

forming bitlines, the bitlines used together with the control gates to read and write from a floating gate,

the direction of the bitlines substantially perpendicular to the direction of the control gates, the floating gates having bitline sides in the bitline direction and control gate sides in the control gate direction;

forming members on the bitline sides of the floating gates, the members shielding the floating gates from electrical fields having a component in the bitline direction.

19. A flash memory device comprising:

floating gates for storing data located above a substrate;

means for isolating adjacent floating gates in the wordline direction;

means for isolating adjacent floating gates in the bitline direction; and

means for reading the data stored in the floating gates, the means for reading the data located above the floating gates and interconnecting strings of floating gates, the means for isolating adjacent floating gates in the bitline direction electrically connected to the means for reading the data.

20. The flash memory device of claim 19 wherein the means for reading the floating gates extends within the means within the substrate for isolating adjacent floating gates.

21. The flash memory device of claim 20 wherein the means for reading shields adjacent floating gates from Yupin effect errors and from disturbs.

22. A method of making a memory device in a substrate comprising:

forming a series of floating gates between a first set of trenches each floating gate having two approximately parallel bitline sides and two approximately parallel roughly rectangular wordline sides;

forming a second set of parallel trenches in an oxide layer deposited within the first set of trenches;

forming a wordline above adjacent floating gates, the wordline extending into the second set of trenches and isolating one of the floating gates from a charge applied at an adjacent floating gate; and

forming a conductive element at each of the approximately parallel bitline sides of the floating gates.

23. The method of claim 22 wherein the conductive elements are located on both sides of a floating gate and wherein the method further comprises electrically contacting the elements to the wordline that selects the floating gate.

24. The method of claim 23 wherein the conductive elements shield a selected floating gate from an electrical field of an adjacent floating gate and minimize field effect coupling in the bitline direction between adjacent floating gates.

25. The method of claim 24 wherein the adjacent floating gate is diagonally adjacent or horizontally adjacent to the selected floating gate and wherein the conductive elements further minimize field effect coupling in the wordline direction.

26. The method of claim 22 wherein the memory device formed is a NAND flash memory device.